UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,063	01/12/2001	Kevin M. Harer	4000/9	2596

35795	7590	06/30/2005

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EXAMINER
STEVENS, THOMAS H

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/760,063	HARER ET AL.
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 May 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-36</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-36</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/25/05</u>.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-36 were examined.

Section I: Response to Applicants' Arguments (2nd Office Action (Final Rejection))

Appendices

2.   Applicants' are thanked for addressing this issue. Objection is withdrawn.

Information Disclosure Statement (IDS)

3.   Examiner acknowledges and accepts IDS dated.

35 USC § 101

4.   Applicants' are thanked for addressing this issue. However, the rejection to this issue stands because the limitation is ambiguous as to who or whom is conducting the post-solution activity. The amended claim, claim 1 for example, states "recording an indication that a goal state has been reached, that can be used by a user, if a goal state has been found; but the specification states (pg. 44, 8-20) "If no new goal state has been identified, at 42 a determination is made, based on a the previous-decided heuristics".

37 CFR 1.132

5.   The affidavit under 37 CFR 1.132 filed 5/25/05 is insufficient to overcome the rejection of claims 1-36 based upon claims as set forth in the last Office action because the declaration lacks technical validity; the evidence is not commensurate with the scope of the claims; and not all inventors presented affidavits.

5a) MPEP 716.01 (c) Although factual evidence is preferable to opinion testimony, such testimony is entitled to consideration and some weight so long as **the opinion is not on the ultimate legal conclusion at issue.** While an opinion as to a legal conclusion is not entitled to any weight, the underlying basis for the opinion may be persuasive. In re Chilowsky, 306 F.2d 908, 134 USPQ 515 (CCPA 1962) (expert opinion that an application meets the requirements of 35 U.S.C. 112 is not entitled to any weight; however, facts supporting a basis for deciding that the specification complies with 35 U.S.C. 112 are entitled to some weight); In re Lindell, 385 F.2d 453, 155 USPQ 521 (CCPA 1967) (Although an affiant's or declarant's opinion on the ultimate legal issue is not evidence in the case, "some weight ought to be given to a persuasively supported statement of one skilled in the art on what was not obvious to him." 385 F.2d at 456, 155 USPQ at 524 (emphasis in original)).

5b) MPEP 2123.01 Applicant's disclosure of his or her own work within the year before the application filing date cannot be used against him or her under 35 U.S.C. 102(a). In re Katz, 687 F.2d 450, 215 USPQ 14 (CCPA 1982) (discussed below). **Therefore, where the applicant is one of the co-authors of a publication cited against his or her application, the publication may be removed as a reference by the filing of affidavits made out by the other authors establishing that the relevant portions of the publication originated with, or were obtained from, applicant.** Such affidavits are called disclaiming affidavits. Ex parte Hirschler, 110 USPQ 384 (Bd. App. 1952). The rejection can also be overcome by submission of a specific declaration by the applicant establishing that the article is describing applicant's own work. In re Katz, 687 F.2d 450, 215 USPQ 14 (CCPA 1982). However, if there is evidence that the co-author has refused to disclaim inventorship and believes himself or herself to be an inventor, applicant's affidavit will not be enough to establish that applicant is the sole inventor and the rejection will stand. Ex parte Kroger, 219 USPQ 370 (Bd. Pat. App. & Int. 1982) (discussed below). It is also possible to overcome the rejection by adding the coauthors as inventors to the application if the requirements of 35 U.S.C. 116, third paragraph are met. In re Searles, 422 F.2d 431, 164 USPQ 623 (CCPA 1970). In In re Katz, 687 F.2d 450, 215 USPQ 14 (CCPA 1982), Katz stated in a declaration that the coauthors of the publication, Chiorazzi and Eshhar, "were students working under the direction and supervision of the inventor, Dr. David H. Katz." The court held that this declaration, in combination with the fact that the publication was a research paper, was enough to establish Katz as the sole inventor and that the work described in the publication was his own. In research papers, students involved only with assay and testing are normally listed as coauthors but are not considered co-inventors. In Ex parte Kroger, 219 USPQ 370 (Bd. Pat. App. & Inter. 1982), Kroger, Knaster and others were listed as authors on an article on photovoltaic power generation. The article was used to reject the claims of an application listing Kroger and Rod as inventors. **Kroger and Rod submitted affidavits declaring themselves to be the inventors. The affidavits also stated that Knaster merely carried out assignments and worked under the supervision and direction of Kroger. The Board stated that if this were the only evidence in the case, it would be established, under In re Katz, that Kroger and Rod were the only inventors. However, in this case, there was evidence that Knaster had refused to sign an affidavit disclaiming inventorship and Knaster had introduced evidence into the case in the form of a letter to the PTO in which he alleged that he was a co-inventor. The**

Board held that the evidence had not been fully developed enough to overcome the rejection. Note that the rejection had

been made under 35 U.S.C. 102(f) but the Board treated the issue the same as if it had arisen under 35 U.S.C. 102(a). See also

case law dealing with overcoming 102(e) rejections as presented in MPEP § 2136.05.

Statements of ownership by Mr. Ho, Mr. Harer and Mr.Damiano, is the only piece of

evidence present in each of their 1.132 affidavits with no other factual technical

evidence thereof. Furthermore each inventor, verbatim, is stating the following:

"disclosing work that originated only from myself and my co-inventors as named", that

fails to answer who is the primary inventor. No affidavits were presented from the other

inventors: Mr. T. Shiple; Mr. J. Kukula; Mr. V. Bertacco and Mr. J. Taylor. (see MPEP

2123.01).

5c) MPEP 716.02 (e) An affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter

with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ

67 (CCPA 1979). "A comparison of the claimed invention with the disclosure of each cited reference to determine the

number of claim limitations in common with each reference, bearing in mind the relative importance of particular

limitations, will usually yield the closest single prior art reference." In re Merchant, 575 F.2d 865, 868, 197 USPQ 785, 787 (CCPA

1978) (emphasis in original). Where the comparison is not identical with the reference disclosure, deviations therefrom should be

explained, In re Finley, 174 F.2d 130, 81 USPQ 383 (CCPA 1949), and if not explained should be noted and evaluated, and if

significant, explanation should be required. In re Armstrong, 280 F.2d 132, 126 USPQ 281 (CCPA 1960) (deviations from example

were inconsequential).

No evidence of technical detail related to the claims was presented.

35 U.S.C. § 102

6.   The examiner is unclear why the attorney is mentioning in his arguments (on

page 12 of 14) example 1 regarding 102(b)/102(e) references when a 102(a) reference

was used in the rejection. Based on the lack of evidence stated in the 1.132 affidavits,

the rejection stands.

35 U.S.C. § 103

7.   Applicants' are thanked for addressing this issue. However, applicants have

argued Appendix 1 is part of the original disclosure and is a proprietary documents.

Examiner acknowledges. However, the applicants have now indicated that the Appendix

1 deleted from prosecution. Since Appendix 1 is now deleted from prosecution,

Appendix 1 now considered as prior art. Furthermore, the applicants stated that

Appendix 1 is proprietary internal document. Examiner finds no notation or disclaimer of

such statement on the document. Subsequently, Appendix 1 issue date of 2/14/00 the is

listed on page 2. Rejection stands.

Section II: (Non-Final Office Action (3rd Office Action (RCE))

Non-Compliant Amendment (37 CFR1.121)

8.   Applicants are reminded of the non-compliant amendment accompanying this

office action since applicants have 30 days or 1 month to replay, whichever is later, to

avoid abandonment.

Claim Rejections - 35 USC § 112

9.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

10.   Claims 1,9,17, and 25 rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter,

one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. Specification doesn't specifically state user's

decision of the goal state condition.

Claim Rejections - 35 USC § 102

11.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (a) the invention was known or used by others in this country, or patented or described in a printed
> publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12.   Claims 1-5, 9-13,17-21,25-29 are rejected under 35 U.S.C. 102 (a) as being

anticipated by Ho et al. ("Smart Simulation Using Collaborative Formal and Simulation

Engines"; IEEE (November 2000)).

Ho et al. teaches a simulation-based functional verification tool which provides

automatic test generation and unreachability analysis (abstract: lines 1-5).

Claim 1: A method of verifying a design for a microcircuit (pg. 120, left column, 3rd

paragraph) the method comprising: beginning random simulation (pg. 120, right

paragraph, lines 4-13) of a sequence of states of a microcircuit design by inputting a

sequence of random input vectors to a random simulation model to obtain a sequence

of random simulation states; monitoring a simulation coverage progress metric to

determine on a basis of said sequence of random simulation states a preference for

beginning formal simulation (pg. 122, left column, lines 1-7) of a sequence of states of

said microcircuit design; beginning formal simulation of a sequence of states of said

microcircuit design by using formal simulation methods to simulate a sequence of formal

simulation (pg. 122, left column, second paragraph) states in a formal simulation model

of said microcircuit design; monitoring a formal coverage progress metric to determine

on a basis of said sequence of formal simulation states a preference for resuming

random simulation of states of said microcircuit design; and resuming said generation of

said random input vector sequence for said random simulation model of a microcircuit

design and said simulating of a sequence of random simulation states of said

microcircuit design caused by inputting said random input vector sequence to said

random simulation model.

Claim 2: The method of Claim 1, wherein said random simulation model and said formal

simulation model are the same (pg.121, right column, 6th paragraph).

Claim 3:The method of Claim 1, wherein said simulating a sequence of formal

simulation states comprises the use of symbolic simulation (pg. 122, left column, 2nd

paragraph, lines 1-16).

Claim 4: The method of Claim 1, wherein said simulating a sequence of formal

simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd

paragraph, lines 20-23).

Claim 5: The method of Claim 1, wherein said simulating a sequence of formal

simulation states comprises the use of symbolic simulation and satisfiability techniques

(pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 9: A method of verifying a design for a microcircuit (pg. 12, left column, 3rd

paragraph), the method performed by a data processing system and comprising:

beginning random simulation (pg. 120, right paragraph, lines 4-13) of a sequence of

states of a microcircuit design by inputting a sequence of random input vectors to a

random simulation model to obtain a sequence of random simulation states; monitoring

a simulation coverage progress metric to determine on a basis of said sequence of

random simulation states a preference for beginning formal simulation of a sequence of

states of said microcircuit design; beginning formal simulation (pg. 122, left column,

lines 1-7) of a sequence of states of said microcircuit design by using formal simulation

methods to simulate a sequence of formal simulation states (pg. 122, left column,

second paragraph) in a formal simulation model of said microcircuit design; monitoring a

formal coverage progress metric to determine on a basis of said sequence of formal

simulation states a preference for resuming random simulation of states of said

microcircuit design (pg. 123, left column, 3rd paragraph, lines 13-19); and resuming said

generation of said random input vector sequence for said random simulation model of a

microcircuit design and said simulating of a sequence of random simulation states of

said microcircuit design caused by inputting said random input vector sequence to said

random simulation model (pg. 123, left column, 3rd paragraph, lines 13-19).

Claim 10: The method of Claim 9, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 11: The method of Claim 9, wherein said simulating a sequence of formal simulation 10 states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 1-16).

Claim 12: The method of Claim 9, wherein said simulating a sequence of formal simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 13: The method of Claim 9, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 17: A data processing system for verifying a design for a microcircuit, the system comprising (pg. 124, right column, 3rd paragraph): a circuit configured for random simulation of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model (pg.120, right paragraph, lines 4-13) to obtain a sequence of random simulation states; a circuit configured for monitoring a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation of a sequence of

states of said microcircuit design; a circuit configured for beginning formal simulation of

a sequence of states of said microcircuit design by using formal simulation methods to

simulate a sequence of formal simulation states (pg. 122, left column, second

paragraph) in a formal simulation model of said microcircuit design; a circuit configured

for monitoring a formal coverage progress metric to determine on a basis of said

sequence of formal simulation states a preference for resuming random simulation of

states of said microcircuit design (pg. 123, left column, 3rd paragraph, lines 13-19); and

a circuit configured for resuming said generation of said random input vector sequence

for said random simulation mode' of a microcircuit design and said simulating of a

sequence of random simulation states of said microcircuit design caused by inputting

said random input vector sequence to said random simulation model.

Claim 18: The system of Claim 17, wherein said random simulation model and said

formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 19: The system of Claim 17, wherein said simulating a sequence of formal

simulation 15 states comprises the use of symbolic simulation (pg. 122, left column, 2nd

paragraph, lines 1-16).

Claim 20: The system of Claim 17, wherein said simulating a sequence of formal

simulation states comprises the use of satisfiability techniques (pg. 122, left column, 2nd

paragraph, lines 20-23).

Claim 21: The system of Claim 17, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 25: A computer program product comprising a computer usable medium having computer readable code embodied therein for verifying a design for a microcircuit, the computer program product comprising (pg. 120, right column, first paragraph): computer readable program code devices configured to cause a computer to effect random simulation of a sequence of states of a microcircuit design by inputting a sequence of random input vectors to a random simulation model to obtain a sequence of random simulation states; computer readable program code devices configured to cause a computer to effect monitoring of a simulation coverage progress metric to determine on a basis of said sequence of random simulation states a preference for beginning formal simulation (pg. 120, right paragraph, lines 4-13) of a sequence of states of said microcircuit design; computer readable program code devices configured to cause a computer to effect beginning formal simulation of a sequence of states of said microcircuit design by using formal simulation methods to simulate a sequence of formal simulation states in a formal simulation model of said microcircuit design; computer readable program code devices configured to cause a computer to effect monitoring a formal coverage progress metric to determine on a basis of said sequence of formal simulation states a preference for resuming random simulation of states of said microcircuit design (pg. 123, left column, paragraphs 2 through 3); and computer

readable program code devices configured to cause a computer to effect resuming (pg. 124, right column, section 4, 1st paragraph) said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design caused by inputting said random input vector sequence to said random simulation model.

Claim 26: The product of Claim 25, wherein said random simulation model and said formal simulation model are the same (pg. 121, right column, 6th paragraph).

Claim 27: The product of Claim 25, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 28: The product of Claim 25, wherein said simulating a sequence of formal simulation 10 states comprises the use of satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim 29: The product of Claim 25, wherein said simulating a sequence of formal simulation states comprises the use of symbolic simulation and satisfiability techniques (pg. 122, left column, 2nd paragraph, lines 20-23).

Claim Rejections - 35 USC § 103

13.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

    1.   Determining the scope and contents of the prior art.

    2.   Ascertaining the differences between the prior art and the claims at issue.

    3.   Resolving the level of ordinary skill in the pertinent art.

14.   Considering objective evidence present in the application indicating obviousness

or nonobviousness.

15.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

    (a) A patent may not be obtained though the invention is not identically disclosed

    or described as set forth in section 102 of this title, if the differences between the

    subject matter sought to be patented and the prior art are such that the subject

    matter as a whole would have been obvious at the time the invention was made

    to a person having ordinary skill in the art to which said subject matter pertains.

    Patentability shall not be negatived by the manner in which the invention was

    made.

16.   Claim 6-8, 14-16, 22-24,30-36 are rejected under 35 U.S.C. 103 (a) as

    unpatentable by Ho et al. ("Smart Simulation Using Collaborative Formal and

    Simulation Engines"; IEEE (November 2000)) in view of Harer ("Design and

Maintenance Specification for CTG Reachability & Control Subsystems"

February 2000). Ho et al. teaches a simulation-based functional verification tool

which provides automatic test generation and unreachability analysis (abstract:

lines 1-5); but doesn't teach injecting a previously simulated process or input

vector. Harer teaches injecting a previously completed simulation process to

obtain the best possible outcome for a predetermine goal. At the time the

invention was made, it would have been obvious to one of ordinary skill in the art

to use Harer to modify Ho et al. solve reachability problems (Harer: pg. 3, section

1.1, 1st paragraph).

Claim 6: The method of Claim 1, wherein said beginning of formal simulation is initiated

by simulating in said formal simulation model (Ho: pg. 122, left column, 2nd paragraph,

lines 1-4) a state of said microcircuit design previously simulated by inputting at least a

portion of said random input vector sequence to said random simulation model (Harer:

pg. 9,instructions 4 and 5).

Claim 7: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4),

further comprising proving at least one of a set of previously-defined goal states of said

microcircuit design unreachable (Harer: pg 9, instruction 8).

Claim 8: The method of Claim 1(Ho: pg. 122, left column, 2nd paragraph, lines 1-4),

wherein said process of monitoring said simulation coverage progress metric, beginning

formal simulation, monitoring said formal coverage progress metric (Ho: pg. 122, left

column, 2nd paragraph, lines 1-4), and resuming said random simulation is continued

until a previously defined set of goal states of said microcircuit design are simulated or

proved not reachable (Harer: pg. 9, instructions 7-10).

Claim 14: The method of Claim 9, wherein said beginning of formal simulation (Ho: pg.

122, left column, 2nd paragraph) is initiated by simulated by inputting at least a portion of

said random input vector sequence to said random simulation model (Harer: pg. 9,

instruction 5).

Claim 15: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), further

comprising proving at least one of a set of previously-defined goal states of said

microcircuit design unreachable (Harer: pg. 9, instructions 6 and 7).

Claim 16: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), wherein said

process of monitoring said simulation coverage progress metric, beginning formal

simulation, monitoring said formal coverage progress metric, and resuming said random

simulation is continued until a previously defined set of goal states of said microcircuit

design are simulated or proved not reachable (Harer: pg. 9, instructions 6-8).

Claim 22: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), wherein

said beginning of formal simulation is initiated by simulating in said formal simulation

model a state of said microcircuit design previously simulated by inputting at least a

portion of said random input vector sequence to said random simulation model (Harer:

pg. 9, instruction 4).

Claim 23: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), further

comprising a circuit configured for proving at least one of a set of previously-defined

goal states of said microcircuit design unreachable (Harer: pg 9, instruction 8).

Claim 24: The system of Claim 17(Ho: pg. 124, right column, 3rd paragraph), wherein

said circuits are configured such that said process of monitoring said simulation

coverage progress metric, beginning formal simulation, monitoring said formal coverage

progress metric (Ho: pg. 122, left column, 2nd paragraph, lines 1-4), and resuming said

random simulation is continued until a previously-defined set of goal states of said

microcircuit design are simulated or proved not reachable (Harer: pg. 9, instructions 7-

10).

Claim 30: The product of Claim 25 (Hop. 120, right column, first paragraph), wherein

said beginning of formal simulation is initiated by simulating in said formal simulation

model a state of said microcircuit design previously simulated by inputting at least a

portion of said random input vector sequence to said random simulation model (Harer:

pg. 9, instructions 6 and 7).

Claim 31: The product of Claim 25 (Ho: pg. 120, right column, first paragraph), further

comprising proving at least one of a set of previously-defined goal states of said

microcircuit design unreachable (Harer: pg. 9, instructions 6-8).

Claim 32: The product of Claim 25 (Ho: pg. 120, right column, first paragraph), wherein

said process of monitoring said simulation coverage progress metric, beginning formal

simulation, monitoring said formal coverage progress metric, and resuming said random

simulation is continued until a previously defined set of goal states of said microcircuit

design are simulated or proved unreachable (Harer: pg. 9, instructions 7-12).

Claim 33: The method of Claim 1 (Ho: pg. 122, left column, 2nd paragraph, lines 1-4),

wherein: said beginning of said formal simulation of a sequence of states is initiated

from a start state; said formal simulation of a sequence of states of said microcircuit

design comprises simulating a state defined as a goal state (Harer: pg. 8, instructions 1-

3); and resuming said generation of said random input vector sequence for said random

simulation model (Harer: pg. 123, left column, 3rd paragraph, lines 13-19) of a

microcircuit design and said simulating of a sequence of random simulation states of

said microcircuit design comprises simulating in said random simulation model a

sequence of states simulated in said formal simulation model, starting with said start

state and comprising said goal state.

Claim 34: The method of Claim 9 (Ho: pg. 12, left column, 3rd paragraph), wherein said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state (Harer: pg. 8, instructions 1-3); and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design arid said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state.

Claim 35: The system of Claim 17(Ho: pg. 12, left column, 3rd paragraph), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start state; said formal simulation of a sequence of states of said microcircuit design comprises simulating a state defined as a goal state; and resuming said generation of said random input vector sequence for said random simulation model of a microcircuit design and said simulating of a sequence of random simulation states of said microcircuit design comprises simulating in said random simulation model a sequence of states simulated in said formal simulation model, starting with said start state and comprising said goal state (Harer: pg 8-9, instructions 1-12).

Claim 36: The product of Claim 25 (Ho: pg. 12, left column, 3rd paragraph), wherein: said beginning of said formal simulation of a sequence of states is initiated from a start

state; said formal simulation of a sequence of states of said microcircuit design

comprises simulating a state defined as a goal state; and resuming said generation of

said random input vector sequence for said random simulation model of a microcircuit

design and said simulating of sequence of random simulation states of said microcircuit

design comprises simulating in said random simulation model a sequence of states

simulated in said formal simulation model, starting with said start state and comprising

said goal state (Harer: pg 8-9, instructions 1-12).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-

3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571)

272-3749. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should

be directed to the TC 2100 Group receptionist: 571-272-2100.

June 22, 2005

THS